Allowed Claims

The Office Action indicates that claim 16 is objected to but allowable if presented in independent form, and claim 17 would be allowable if amended to overcome the rejection under 35 U.S.C. §112, second paragraph. Applicants submit that all of the claims are in immediate condition for allowance for the reasons set forth below and in view of the above amendments.

Claim Objection

Claims 11, 19 and 25 were objected to for informalities. In this response, claims 11, 19 and 25 have been amended according to the Examiner's helpful instructions. Thus, withdrawal of the objection is respectfully solicited.

35 U.S.C. §112 Rejection

Claims 14, 15 and 17-20 have been rejected under 35 U.S.C. §112, second paragraph. This rejection is respectfully traversed.

In claims 14 and 15, the terminology "unused chip pads" has been amended to "unused pads". The first occurrence of "unused pads" is not designated with "the" or "said", and the second occurrence "unused pads" are properly designated with "said". Thus, claims 14 and 15 do not cause any antecedent basis issues.

In claim 17, the first occurrences of "power rails", "power return rails" and "at least two different power supplies" are not provided with "the" or "said", and thus do not cause any antecedent basis issues. In claim 18, the recitation of "I/O cells to I/O cells to an I/O pad" is replaced with -- I/O cells to an I/O pad".

Accordingly, withdrawal of the rejection under 35 U.S.C. §112, second paragraph is respectfully requested.

35 U.S.C. §102 Rejections

Claims 7-8, 11-13, 18, 20-22, 25 and 26 were rejected under 35 U.S.C. §102(a) for being anticipated by a technical article by Zuchowski ("Zuchowski"). Claims 13, 18 and 19 have been rejected under 35 U.S.C. §102(e) for being anticipated by U. S. Patent No. 5,689,432 to Blaauw, et al. ("Blaauw"). Claims 7, 8, 11-13, 18, 19, 21, 22, 25 and 26 were rejected under 35 U.S.C.

§102(e) for being anticipated by U. S. Patent No. 5,648,910 to Ito ("Ito"). Claims 7, 8, 11-13, 18-22 and 25-26 were rejected under 35 U.S.C. §102(e) for being anticipated by U. S. Patent No. 5,796,638 to Kang, et al. ("Kang"). These rejections are respectfully traversed.

Independent claim 13 has been amended to incorporate all the limitations of its allowable dependent claim 16. Independent claims 7, 18 and 21 are amended to further include the subject matter recited in allowable claims 16 and/or 17. Accordingly, Applicants submit that these rejections are moot and that the rejections under 35 U.S.C. §102 be withdrawn.

Claim Rejection Under 35 U.S.C. §103

Claims 9, 14 and 23 were rejected under 35 U.S.C. §103(a) over Zuchowski or Ito or Kang or Blaauw in view of U. S. Patent No. 5,155,065 to Schweiss, *et al.* ("Schweiss"). Also, claims 10, 15 and 24 were rejected under 35 U.S.C. §103(a) over Zuchowski or Ito or Kang or Blaauw in view of U. S. Patent No. 6,043,539 to Sugasawara ("Sugasawara"). These rejections are respectfully traversed.

Claims 9, 10, 14, 15, 23 and 24 are dependent claims from claims 7, 13 and 21, respectively. Independent claims 7, 13 and 21 have been amended to include allowable subject matter. Thus, claims 9, 10, 14, 15, 23 and 24 would be also patentable at least for the same reason. Accordingly, Applicants respectfully request that the §103 rejections be withdrawn.

Other Matters

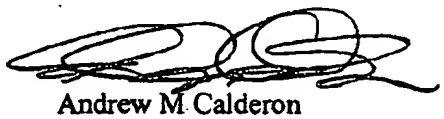
In this response, claims 7, 9-15 and 17-26 have been amended to correct informalities.

CONCLUSION

Applicants appreciate the indication of allowable subject matter. In view of the foregoing, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the local telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required.

Please charge any deficiencies and credit any overpayment of fees to Deposit Account No. 23-1951 (McGuireWoods).

Respectfully submitted,



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APPENDIX A

Please amend the claims, as follows. The entire set of the pending claims, including the clean version of the amended claims, is provided in the APPENDIX B.

7. (Amended) A chip design method comprising the steps of:

a) retrieving a wire width constraint from technology data for an I/O cell of a chip;

b) retrieving a maximum resistance constraint from said technology data for said I/O cell;

c) propagating said wiring width constraint and said maximum resistance constraint to net design data for said chip;

d) generating said chip, comprising the steps of:

constraining connections between said I/O cell and an associated pad [being constrained] by said propagated constraints; [and,]

providing a plurality of ESDxx cells; and

connecting said plurality of ESDxx cells between power rails and power return rails for at least two different power supplies; and

e) checking said wired integrated circuit.

9. (Amended) The method of claim 8, further comprising before the checking step (e), the step of[: d1)] wiring any unused chip pads to [a cell] one of said I/O cells including a connection to said power [rail] rails or to [a] said power return [rail] rails.

10. (Amended) The method of claim 8, further comprising before the checking step (e), the step of[: d1)] wiring any unused chip pads to [a cell including an ESD protect device] one of said ESDxx cells.

11. (Amended) The method of claim 8, wherein the generating step (d) comprises the [step] steps of:

i) placing each of said IO cells based on said propagated wire width and maximum resistance constraints; and

ii) routing a connection between each said placed I/O cell and its said associated pad, each said routed connection meeting said propagated wire width and maximum resistance constraints.

12. (Amended) The method of claim 11, where the checking step (e) comprises checking connections made in said generating step (d) against said propagated wire width and maximum resistance constraints.

13. (Amended) A chip design method comprising the steps of:

a) retrieving a power route pattern instruction;

b) identifying power and power return connections;

c) routing each said power and each said power return connection, each said routed connection meeting wire width and maximum resistance constraints in said retrieved power route pattern instruction, wherein the routing step includes the steps of:

i) providing an ESDxx cell; and

ii) connecting said ESDxx cell between power rails and power return rails for at least two different power supplies; and

d) checking said wired integrated circuit.

14. (Amended) The method of claim 13, wherein the routing step (c) further includes the step of identifying [any] unused [chip] pads and wiring said unused pad to [a] said power rails or to [a] said power return rails.

15. (Amended) The method of claim 13, wherein the routing step (c) further includes the step of identifying [any] unused [chip] pads and wiring said unused pad to a cell including an ESD protect device.

16. Cancelled

17. (Amended) A chip design method comprising the steps of:

a) retrieving [I/O and ESDxx cell] identifications and placement constraints of a plurality of I/O cells and a plurality of ESDxx cells;

b) providing said plurality of I/O cells [a plurality of ESDxx cells] for placement according to said placement constraints;

c) placing each of said plurality of ESDxx cells with [a group] said plurality of I/O cells;

d) connecting each of said placed ESDxx [cell] cells between power rails and power return rails for at least two different power supplies; and[,]

e) checking said wired integrated circuit.

18. (Amended) A system for integrated circuit chip design comprising:

means for retrieving net constraints from technology data;

means for placing a plurality of I/O cells; [and]

means for placing a plurality of ESDxx cells;

means for connecting each of said placed I/O cells [to I/O cells] to an I/O pad according to said retrieved net constraints; and

means for connecting said placed ESDxx cells between power rails and power return rails for at least two different power supplies.

19. (Amended) The system of claim 18, wherein said retrieved [constrains] constraints include power bussing constraints, said system further comprising[:] means for routing power and power return connections according to said power bussing constraints.

20. (Amended) The system of claim 18, further comprising:

means for grouping I/O cells; and

means for placing [an] said plurality of ESDxx [cell] cells with [each group of] said grouped I/O cells.

21. (Amended) A computer readable medium comprising instructions for a computer implemented chip design method, said method comprising the steps of:

a) retrieving a wire width constraint from technology data for an I/O cell;

b) retrieving a maximum resistance constraint from said technology data for said I/O cell;

c) propagating said wiring width constraint and said maximum resistance constraint to net design data for said chip;

d) generating said chip, comprising the steps of:

constraining connections between said I/O cell and an associated pad [being constrained] by said propagated constraints; [and,]

providing a plurality of ESDxx cells; and

connecting said plurality of ESDxx cells between power rails and power return rails for at least two different power supplies; and

e) checking said wired integrated circuit.

23. (Amended) The computer readable medium comprising instructions as recited in claim 22, further comprising before the checking step (e), the step of [: d1)] wiring any unused chip pads to [a cell] one of said I/O cells including a connection to power rail or to a power return rail.

24. (Amended) The computer readable medium comprising instructions as recited in claim 22, further comprising before the checking step (e), the step of[: d1)] wiring any unused chip pads to one of said ESDxx cells [a cell including an ESD protect device].

25. (Amended) The computer readable medium comprising instructions as recited in claim 22, wherein the generating step (d) comprises the [step] steps of:

i) placing each of said I/O cells based on said propagated wire width and maximum resistance constraints; and

ii) routing a connection between each said placed I/O cell and its said associated pad, each said routed connection meeting said propagated wire width and maximum resistance constraints.

26. (Amended) The computer readable medium comprising instructions as recited in claim 25, wherein the checking step (e) comprises the step of checking connections made in said generating step (d) against propagated wire width and maximum resistance constraints.

APPENDIX B

The entire set of the pending claims, including the clean version of the amended claims, is as follows.

7. (Amended) A chip design method comprising the steps of:

a) retrieving a wire width constraint from technology data for an I/O cell of a chip;

b) retrieving a maximum resistance constraint from said technology data for said I/O cell;

c) propagating said wiring width constraint and said maximum resistance constraint to net design data for said chip;

d) generating said chip, comprising the steps of:

constraining connections between said I/O cell and an associated pad by said propagated constraints;

providing a plurality of ESDxx cells; and

connecting said plurality of ESDxx cells between power rails and power return rails for at least two different power supplies; and

e) checking said wired integrated circuit.

8. The method of claim 7, wherein a plurality of I/O cells are wired and further comprising before the checking step (e), repeating steps (a) - (d) for each of said plurality of I/O cells.

9. (Amended) The method of claim 8, further comprising before the checking step (e), the step of wiring any unused chip pads to one of said I/O cells including a connection to said power rails or to said power return rails.

10. (Amended) The method of claim 8, further comprising before the checking step (e), the step of wiring any unused chip pads to one of said ESDxx cells.

11. (Amended) The method of claim 8, wherein the generating step (d) comprises the steps of:

i) placing each of said IO cells based on said propagated wire width and maximum resistance constraints; and

ii) routing a connection between each said placed I/O cell and its said associated pad, each said routed connection meeting said propagated wire width and maximum resistance constraints.

12. (Amended) The method of claim 11, where the checking step (e) comprises checking connections made in said generating step (d) against said propagated wire width and maximum resistance constraints.

13. (Amended) A chip design method comprising the steps of:

a) retrieving a power route pattern instruction;

b) identifying power and power return connections;

c) routing each said power and each said power return connection, each said routed connection meeting wire width and maximum resistance constraints in said retrieved power route pattern instruction, wherein the routing step includes the steps of:

i) providing an ESDxx cell; and

ii) connecting said ESDxx cell between power rails and power return rails for at least two different power supplies; and

d) checking said wired integrated circuit.

14. (Amended) The method of claim 13, wherein the routing step (c) further includes the step of identifying unused pads and wiring said unused pad to said power rails or to said power return rails.

15. (Amended) The method of claim 13, wherein the routing step (c) further includes the step of identifying unused pads and wiring said unused pad to a cell including an ESD protect device.

16. Cancelled

17. (Amended) A chip design method comprising the steps of:

a) retrieving identifications and placement constraints of a plurality of I/O cells and a plurality of ESDxx cells;

b) providing said plurality of I/O cells for placement according to said placement constraints;

c) placing each of said plurality of ESDxx cells with said plurality of I/O cells;

d) connecting each of said placed ESDxx cells between power rails and power return rails for at least two different power supplies; and

e) checking said wired integrated circuit.

18. (Amended) A system for integrated circuit chip design comprising:

means for retrieving net constraints from technology data;

means for placing a plurality of I/O cells;

means for placing a plurality of ESDxx cells;

means for connecting each of said placed I/O cells to an I/O pad according to said retrieved net constraints; and

means for connecting said placed ESDxx cells between power rails and power return rails for at least two different power supplies.

19. (Amended) The system of claim 18, wherein said retrieved constraints include power bussing constraints, said system further comprising means for routing power and power return connections according to said power bussing constraints.

20. (Amended) The system of claim 18, further comprising:

means for grouping I/O cells; and

means for placing said plurality of ESDxx cells with said grouped I/O cells.

21. (Amended) A computer readable medium comprising instructions for a computer implemented chip design method, said method comprising the steps of:

a) retrieving a wire width constraint from technology data for an I/O cell;

b) retrieving a maximum resistance constraint from said technology data for said I/O cell;

c) propagating said wiring width constraint and said maximum resistance constraint to net design data for said chip;

d) generating said chip, comprising the steps of:

constraining connections between said I/O cell and an associated pad by said propagated constraints;

providing a plurality of ESDxx cells; and

connecting said plurality of ESDxx cells between power rails and power return rails for at least two different power supplies; and

e) checking said wired integrated circuit.

22. The computer readable medium comprising instructions as recited claim 21, wherein a plurality of I/O cells are wired and further comprising before the checking step (e), repeating steps (a) - (d) for each of said plurality of I/O cells.

23. (Amended) The computer readable medium comprising instructions as recited in claim 22, further comprising before the checking step (e), the step of wiring any unused chip pads to one of said I/O cells including a connection to power rail or to a power return rail.

24. (Amended) The computer readable medium comprising instructions as recited in claim 22, further comprising before the checking step (e), the step of wiring any unused chip pads to one of said ESDxx cells.

25. (Amended) The computer readable medium comprising instructions as recited in claim 22, wherein the generating step (d) comprises the steps of:

i) placing each of said I/O cells based on said propagated wire width and maximum resistance constraints; and

ii) routing a connection between each said placed I/O cell and its said associated pad, each said routed connection meeting said propagated wire width and maximum resistance constraints.

26. (Amended) The computer readable medium comprising instructions as recited in claim 25, wherein the checking step (e) comprises the step of checking connections made in said generating step (d) against propagated wire width and maximum resistance constraints.